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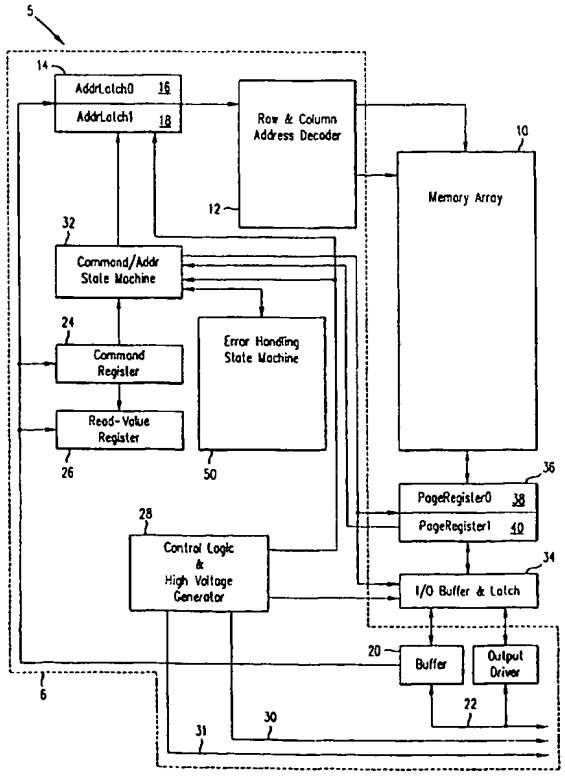
(54) Title: METHOD AND APPARATUS FOR MEMORY CONTROL CIRCUIT

(57) Abstract

A method and circuit for fast memory access (read or write) of the data to and from a memory array is disclosed. Architecture wise, the memory array control circuit (5) provides for at least two address latches and two page registers. The first address latch (16) contains a first data address and the second address latch (18) contains a second data address. The first data address is decoded first and sent to the memory array (10) to access (read or write) the corresponding data from the memory array (10). When the data of the first data address is being accessed, the decoding process will begin for a second data address. When the data of the first data address has been accessed, the second data address is ready for the memory array. Thus, there can be continuous fetching from or writing to the memory array (10). In the preferred embodiment, there are two page registers (38, 40). In a read operation, the data read from the first data address is transferred to a first page register (38). When the data of the second data address is being accessed, the data in the first page register (38) is transferred to a second page register (40). When the operation to read the data from the second data address is completed, the data can be placed in the first register (38). The data in the second page register can be rapidly transferred to a latch and on to a bus. In this manner, there is always space made available for the data read. Similarly, in a write operation, data is transferred from the data bus to the second page register and then to the first page register. The data in the first register is written into the memory array.



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Specification

METHOD AND APPARATUS FOR MEMORY CONTROL CIRCUIT

Referenced to Prior Application

This application claims the benefit of previously filed U.S. Provisional Application No. 60/108,872 filed November 17, 1998, and entitled "METHOD AND APPARATUS FOR MEMORY CONTROL CIRCUIT."

Field of the Invention

The present invention generally relates to nonvolatile memory arrays, and, in particular, to control circuits for increasing the speed of operations performed on the nonvolatile memory arrays.

BACKGROUND OF THE INVENTION

In the conventional method of accessing memory arrays (including flash memory arrays), whether it be a read or write operation, each operation is performed sequentially, meaning that an operation has to be completed before the start of the next read or write operation. In performing an operation to access a memory array, the given data address is first decoded and the decoded address is provided to the memory array for fetching the data or storing the data. Because each of the decoding and accessing steps are done in a sequential manner, these architectures of the prior art memory arrays do not lend themselves to faster throughputs necessary for modern day high-speed memory access and throughput requirements.

Timing diagrams exemplifying prior art techniques are shown in Figs. 3(a) and 3(b) and will be discussed in more detail later. Briefly, these prior art methods and systems require overhead time for shifting the data into a temporary storage location prior to storing the same in nonvolatile or flash memory for and during each write command. In fact, the next write command cannot begin prior to the completion of the tasks associated with performing a write command. Thus, system efficiency suffers where many write operations need be performed, as is the case in most memory systems.

Therefore, it would be desirable to have a method and memory architecture conducive to high-speed memory throughput not limited to the sequential speed of each memory access.

SUMMARY OF THE INVENTION

It is the object of the present invention to provide a method and architecture for high speed accessing of a memory array with respect to write-to-memory and read-from-memory operations.

It is another object of the present invention to provide a method and architecture for high speed accessing of a memory array that allows for continuous read or write operations from and to the memory array.

It is yet another object of the present invention to provide a method and architecture for high speed accessing of a memory array, which allows for continuously decoding of data addresses for reading or writing from and to the memory array.

It is still another object of the present invention to provide a method and architecture, which allows for the decoding of a data address while the data addressed by the previous data address is being accessed.

Briefly, the presently preferred embodiment of the present invention provides a method and architecture for fast memory access (read or write) of the data to and from a memory array. Architecture wise, the memory array control circuit provides for at least two address latches and two page registers. The first address latch contains a first data address and the second address latch contains a second data address. The first data address is decoded first and sent to the memory array to access (read or write) the corresponding data from the memory array. When the data of the first data address is being accessed, the decoding process will begin for a second data address. When the data of the first data address has been accessed, the second data address is ready for the memory array. Thus, there can be continuous fetching from or writing to the memory array. In the preferred embodiment, there are two page registers. In a read operation, the data read from the first data address is transferred to a first page register. When the data of the second data address is being accessed, the data in the first page register is transferred to a second page register. When the operation to read the data from the second data address is completed, the data can be placed in the first register. The data in the second page register can be rapidly transferred to a latch and on to a bus. In this manner, there is always space made available for the data read. Similarly, in a write operation, data is transferred from the data bus to the second page register and then to the first page register. The data in the first register is written into the memory array.

An advantage of the present invention is that it provides a method and architecture for high speed accessing of a memory array with respect to write-to-memory and read-from-memory operations.

Another advantage of the present invention is that it provides a method and architecture for high speed accessing of a memory array that allows for continuous read or write operations from and to the memory array.

Yet another advantage of the present invention is that it provides a method and architecture for high speed accessing of a memory array, which allows continuously decoding of data addresses for reading or writing from and to the memory array.

Still yet another advantage of the present invention is that it provides a method and architecture, which allows for the decoding of a data address while the data addressed by the previous data address is being accessed.

These and other features and advantages of the present invention will become well understood upon examining the figures and reading the following detailed description of the invention.

IN THE DRAWINGS

Fig. 1 is a block diagram illustrating the host, the memory controller and a memory circuit.

Fig. 2 is a detailed block diagram illustrating the memory circuit.

Figs. 3a and 3b illustrate prior art timing diagrams for a write operation.

Figs. 4a and 4b illustrate timing diagrams for a write operation using the preferred embodiment of the present invention.

Figs. 5a and 5b illustrate prior art timing diagrams for a read operation.

Figs. 6a and 6b illustrate timing diagrams for a read operation using the preferred embodiment of the present invention.

Fig. 7 is a flow chart illustrating the steps in writing to the memory array.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The description provided herein makes references to a flash (or nonvolatile, which may be other than flash, such as EEPROM) memory array. However, it shall be understood that the present invention may be used in any memory architecture. Referring now to Fig. 1, a host 101 interfaces with a flash memory controller 100 in storing and retrieving digital information, in the form of user data or other kind of data, to and from a flash memory

circuit 102. The controller 100 is generally comprised of a circuit for coding and decoding error correction code (ECC) 104, a flash state machine 106, a flash controller 108, a host interface 105 for communicating with the host, a SPM controller/state machine 109, SPM RAM 110, RAM 111, ROM 112, a microprocessor 113 and a data buffer RAM 103. The data buffer RAM 103 is used for temporary storage of information prior to a more permanent storage of or after reading information from the flash memory circuit 102.

Referring now to Fig. 2, a flash memory circuit 5 is shown to include a flash memory cell array 10 and control circuitry 6 for operating the flash memory cell array 10 in accordance with an embodiment of the present invention. The control circuitry 6 includes a row and column address decoder 12, an address double latch 14, a buffer 20, a command register 24, a read-value register 26, a control logic unit 28, a state machine 32, an I/O buffer and latch 34, a double data latch 36 (which includes a PageRegister 0 38 and a PageRegister 1 40), an output driver 21 and an error handling state machine 50.

The flash memory cell array 10 includes flash memory cells that are addressable by row and column address signals provided by the row and column address decoder 12. The row and column address decoder 12 receives addresses from the address double latch 14. The double latch 14 is comprised of two latches, an AddrLatch0 16 and an AddrLatch1 18. The double address latch 14 receives its input from the buffer 20, which, in turn, receives its input from an I/O bus 22. The buffer 20 also provides signals to the command register 24 and the read-value register 26. The control logic unit 28 in response to input signals (ready signal and command/address control lines received at 30 and 31), and working in conjunction with the state machine 32 operates the buffer 20, I/O buffer and latch 34, and the double data latch 36. The double data latch 36 is comprised of PageRegister0 38 and PageRegister1 40 and sends (or writes) and/or receives (reads) data to and from the flash memory array 10. An error handling state machine 50 handles errors occurring in the writing to the memory array 10.

In operation, the controller (Fig. 1, 100) sends and receives 512 bytes of data (or as otherwise specified) plus error correction code (ECC) and address information to and from the flash memory circuit (Fig. 2, 102). When the controller sends (or writes) data to the flash memory circuit, the flash memory circuit latches the data to be written into a PageRegister (PageRegister0 38 or PageRegister1 40 in Fig. 2) and starts the write operation to the flash memory array 10. At this time the flash memory circuit (Fig. 1, 102) asserts a Ready/Busy signal, which is monitored by the controller (Fig. 1, 100) as to whether the flash

memory circuit has completed the write operation. Once the controller (Fig. 1, 100) detects the end of the write operation, it reads the status register to check for any error conditions. If there was no error, the controller starts a new write operation by sending a new write command followed by new data.

In the present invention, a new write command and data is sent to the flash memory circuit while the previous data is being written the flash memory array. This has a pipelining effect. By pipelining the data, no time is lost in waiting for the completion of the previous write operation. The error handling state machine 50 is provided to handle errors occurring from the write operation thus relieving the controller from handling the errors.

In a read operation, the row and column address decoder 12, in response to an address received from AddrLatch0 or AddrLatch1, decodes the address, and provides the decoded address to the flash memory cell array 10. Data is then read from a location within the flash memory cell array 10 that is identified by the decoded address. The data that is read is then provided to the PageRegister0 38. In a write operation, an address from AddrLatch0 or AddrLatch1 is provided to the row and column address decoder 12 to activate the corresponding address(es) in the flash memory cell array 10. The data to be written to the flash memory cell 10 is provided by the PageResister0 38 or PageRegister1 40.

One of the advantages of the present invention is that during a first time period the address can be read from AddrLatch0 16 to initiate the operation to write the data from PageRegister0 38. At the same time, a new address can be written to AddrLatch1 18 and a new data word can be written to PageRegister1 40. During a second time period, the address can be read in from AddrLatch1 and data can be read from PageRegister1 40. Moreover, a new address can be written to AddrLatch0 16 and the new data word can be written to PageRegister0 38. In this manner, a ping-pong effect is achieved where while a first set of address and data pair is being written to the flash memory array 10 a second set of address and data pair is being written to the corresponding address latch and page register for the next write operation. In an alternate embodiment, a first-in-first-out (FIFO) method can be implemented rather than a ping-pong method.

More specifically, in operation, when the flash memory apparatus receives a write command, the address is shifted into AddrLatch0 16 and the corresponding data to be written is shifted into PageRegister0 38, and the data is then written to the corresponding flash memory cell array 10. During this period, the controller (Fig. 1, 100) determines if

there is another write command pending from the host. If there is another write command pending, the address for the new data is shifted into AddrLatch1 18 and the corresponding new data is shifted into PageRegister1 40. At the end of the first write command, the command/address state machine 32 checks error status to verify successful completion of the write command. If the write command was completed successfully, the command pending flag is checked. If there is a command pending and a new word of data is received at the alternate PageRegister1 40, data in PageRegister1 40 is written to the flash memory cell array 10. In this manner, a ping-pong effect is achieved where while data in one PageRegister is being written to the flash memory cell array, another word of data is being loaded into the alternate PageRegister in preparation for writing during the next time period. This process continues until no new data is to be written to the flash memory array or an error condition occurred. This process eliminates the overhead time required for shifting the data into the PageRegister for each write command.

Figs. 3a and 3b illustrate a prior art timing diagram and Figs. 4a and 4b illustrate the timing diagram showing the elimination of the overhead time required for loading data into the PageRegister. Fig. 3a illustrates the state of the I/O bus where there is a command phase followed by a address phase followed by a data phase and a break for writing the data into the flash memory array. At the end of the first write cycle, the error status is checked (read status phase indicated at 52) to ensure successful completion of the write cycle. Fig. 3b illustrates the state of the ready signal where the bus is available during time t1 but is not being used. Fig. 4a illustrates the state of the I/O bus where there is not a break after a command/address/data phase. Instead, it is immediately followed by another command/address/data phase to load AddrLatch0 or AddrLatch1 and PageRegister0 or PageRegister1. The state of the ready signal is illustrated in Fig. 4b. In this setup, the end of the first write operation occurs in time as indicated at 54 and the end of the second write operation occurs in time as indicated at 56. There is a phase (58) for reading the status for the completion of the write operation. In this manner, a faster throughput is achieved by using the previous write-to-array-time for loading of another address/data into the respective registers (ping-pong).

During a read operation, the flash memory circuit receives a read command causing the requested data to be read from the flash memory array to PageRegister0 and transferred to PageRegister1 (similar to a FIFO). The data now on PageRegister1 is sent to the controller (requester). As the data is being transferred from PageRegister1 to the controller

via the I/O bus, the Command/Address state machine starts a new read operation where the data read is shifted to PageRegister0. When the controller finishes receiving the data from PageReegister1, the content of PageRegister0 is transferred to PageRegister1 and sent to the controller.

The command/add state machine checks if the number of read has been achieved by looking at the value in the read-value register. The value in this register is loaded by the controller before the start of the read command to indicate the number of read operation requested.

Fig. 5a illustrates the prior art approach showing the state of I/O bus where there is a read command phase followed by an address phase and a waiting period for the data to be read from the flash memory array before it is shifted on to the bus. This cycle is followed by another waiting period before data can be shifted on to the bus. Fig. 5b illustrates the state of the ready signal. Fig. 6a illustrates the state of the I/O bus under the preferred embodiment where a read command phase is followed by an address phase and a waiting period for reading of the first data. After the first word of data is read, it can be shifted on to the bus. When the data is being transferred to the controller, the next data word is read from the flash memory array. In this manner, data can be rapidly transferred from the memory on to the bus. Fig. 6b illustrates the state of the ready signal where the timing for starting the reading operation for the next word of data is indicated at 60.

In an alternate embodiment, a first latch can be put in place selectively connect PageRegister0 or PageRegister1 to the flash memory array and a second latch can be put into place to selectively connect PageRegister0 and PageRegister1 to the I/O bus. In this manner, maximum flexibility can be afforded in operating this circuit.

Fig. 7 illustrates the operating steps in a write operation. Here, in the first step 200, a write command is received and the command is decoded 202. The received data is shifted into an available PageRegister 204 and the write to memory array operation is initiated 206. The write operation is constantly checked for completion 208. Once the operation is completed, the logic checks for errors in the write operation 210. If there is an error in the write operation, the appropriate status register is set 212. At the same time the memory array is being written, the logic checks for the existence of a subsequent write operation. If there is another pending write operation, it is processed in the same manner where the logic flows back to step 202.

Although the present invention has been described in terms of specific embodiments it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alterations and modifications as fall within the true spirit and scope of the invention.

What I claim is:

CLAIMS

1. A nonvolatile memory control circuit for controlling reading and writing operations to and from a nonvolatile memory array, comprising:

a set of page registers having at least a first page register and a second page register for buffering data that is to be written to or read from a nonvolatile memory array; said control circuit for receiving commands to operate said set of page registers for reading from and writing to said nonvolatile memory array,

wherein during a current write command, data corresponding to the current write command is stored in said second page register while data corresponding to a previous write command is stored in the nonvolatile memory array from the first page register thereby creating a pipe-lining affect so as to expedite the performance of write operations to the nonvolatile memory array.

2. A nonvolatile memory control circuit as recited in claim 1 including a set of address latches coupled to the nonvolatile memory array, said set of address latches having at least a first address latch and a second address latch for receiving data addresses for addressing the nonvolatile memory array.

3. A nonvolatile memory control circuit as recited in claim 2 wherein during a first time period, said control circuit operates said set of address latches to have a first data address from said first address latch decoded for a read operation.

4. A nonvolatile memory control circuit as recited in claim 3 wherein, in a second time period, data read from said first data address of said memory array is fetched and placed in said first page register.

5. A nonvolatile memory control circuit as recited in claim 4 wherein said control circuit, in a second time period, operates said set of address latches to have a second data address from said second address latch decoded for a read operation.

6. A nonvolatile memory control circuit as recited in claim 4 wherein, in said second time period, data in said first page register is transferred to a bus.

7. A nonvolatile memory control circuit as recited in claim 5 wherein, in a third time period, data read from said second data address of said nonvolatile memory array is fetched and placed in said second page register.

8. A nonvolatile memory control circuit as recited in claim 2 wherein said control circuit, in a first time period, operates said set of address latches to have a first data address from said first address latch decoded for a write operation.

9. A nonvolatile memory control circuit as recited in claim 8 wherein said control circuitry, in said first time period, causes said first page register to store data to be stored in said memory array.

10. A nonvolatile memory control circuit as recited in claim 8 wherein, in a second time period, data stored in said first page register is placed in the nonvolatile memory array.

11. A nonvolatile memory control circuit as recited in claim 9 wherein said control circuit, in a second time period, operates said set of address latches to have a second data address from said second address latch decoded for a write operation.

12. A nonvolatile memory control circuit as recited in claim 11 wherein said control circuit, in said second time period, causes said second page register to store data to be stored in the nonvolatile memory array.

13. A nonvolatile memory control circuit as recited in claim 2 further comprising:

a state machine for operating said set of page registers and said address latches;

an address decoder for receiving and decoding data addresses to the nonvolatile memory array; and

a state machine control logic for operating said state machine in response to received commands.

14. A nonvolatile memory control circuit as recited in claim 13 further comprising an error handling state machine for handling error conditions in accessing the nonvolatile memory array.

15. A method for reading from a nonvolatile memory array, comprising the steps of:

decoding during a first time period a received first data address;

fetching during a second time period data stored at said decoded first data address of said memory array and storing said fetched data in a first page register;

decoding during said second time period a received second data address;

fetching during a third time period data stored at said decoded second data address of said memory array and storing said fetched data in a second page register;

transferring during said third time period data stored in said first page register to a designated location; and

decoding during said third time period a received third data address.

16. A method of claim 15 further including the steps of:

fetching during a fourth time period data stored at said decoded third data address of said memory array and storing said fetched data in said first page register;

transferring during said fourth time period data stored in said second page register to said designated location; and

decoding during said fourth time period a received fourth data address.

17. A method for writing from a memory array, comprising the steps of:

decoding during a first time period a received first data address;

placing, during a second time period, data stored in a first page register into a memory array;

decoding during said second time period a received second data address;

transferring, during said second time period, data from a pre-designated source into a second page register;

placing, during a third time period, data stored in said second page register into said memory array;

transferring, during said third time period, data from said pre-designated source into said first page register; and

decoding during said third time period a received third data address.

18. A nonvolatile memory control circuit for controlling reading and writing operations to and from a nonvolatile memory array, comprising:

a set of page registers coupled to a nonvolatile memory array, said set of page registers having at least a first page register and a second page register for buffering data that is to be written to or read from the nonvolatile memory array; said control circuit for receiving commands to operate said set of page registers for reading from and writing to the nonvolatile memory array,

control circuitry coupled to said set of page registers and the nonvolatile memory array wherein during a current write command, data corresponding to said write command is stored in said second page register while data corresponding to a previous write command is being stored in the nonvolatile memory array from the first page register thereby creating a pipe-lining affect to expedite performing write operations on the nonvolatile memory array.

19. A nonvolatile memory control circuit as recited in claim 18 wherein said control circuitry includes a set of address latches coupled to the nonvolatile memory array, said set of address latches having at least a first address latch and a second address latch for receiving data addresses for addressing the nonvolatile memory array.

20. A nonvolatile memory control circuit as recited in claim 19 wherein said control circuitry further includes,

a state machine for operating said set of page registers and said address latches;

an address decoder for receiving and decoding data addresses to the nonvolatile memory array; and

a state machine control logic for operating said state machine in response to received commands.

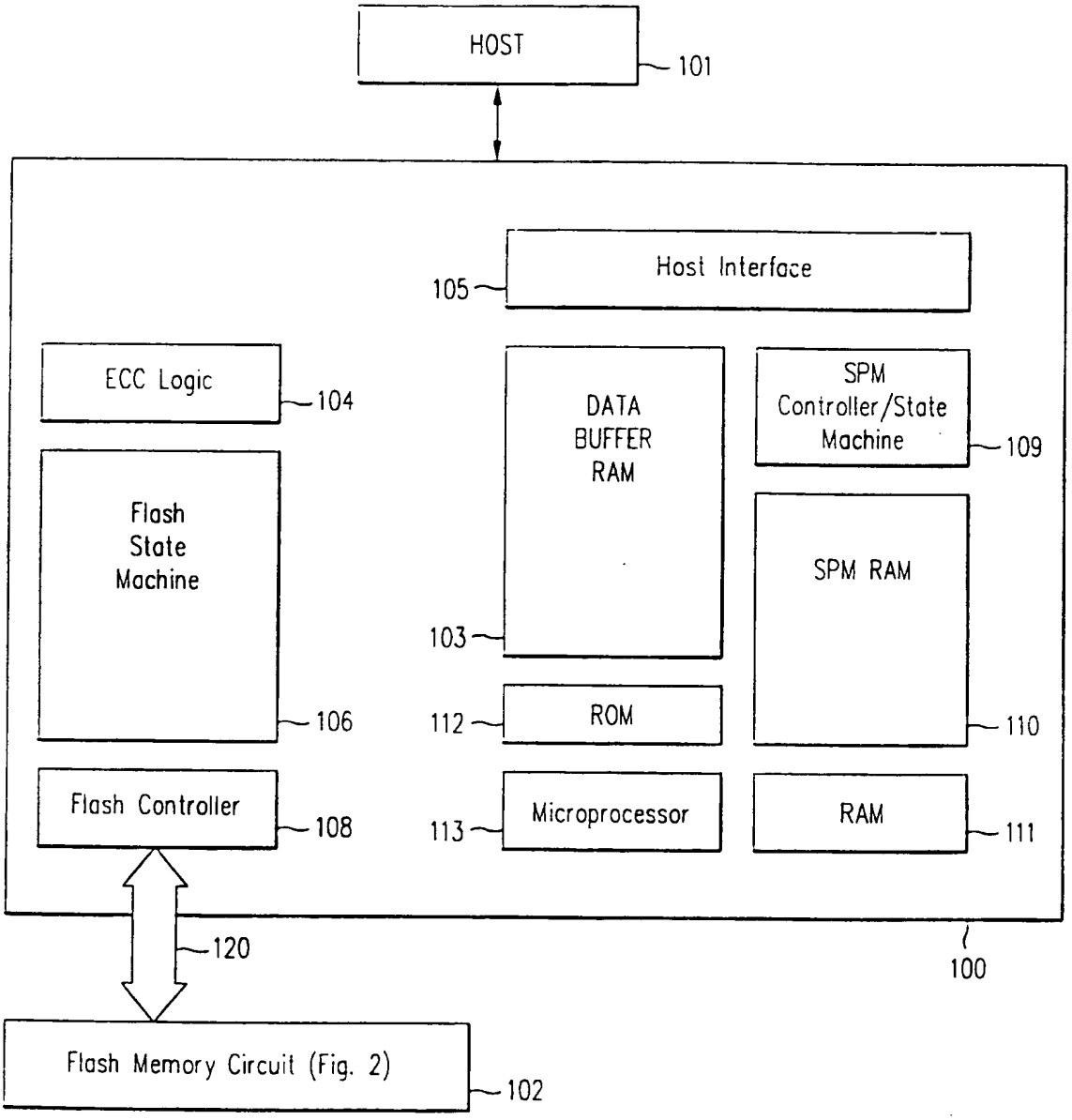
HOST
101
105
Host Interface
ECC Logic
104
DATA
BUFFER
RAM
SPM
Controller/State
Machine
109
Flash
State
Machine
SPM RAM
103
112
ROM
106
110
Flash Controller
108
113
Microprocessor
RAM
111
120
100
Flash Memory Circuit (Fig. 2)
102

FIG. 1

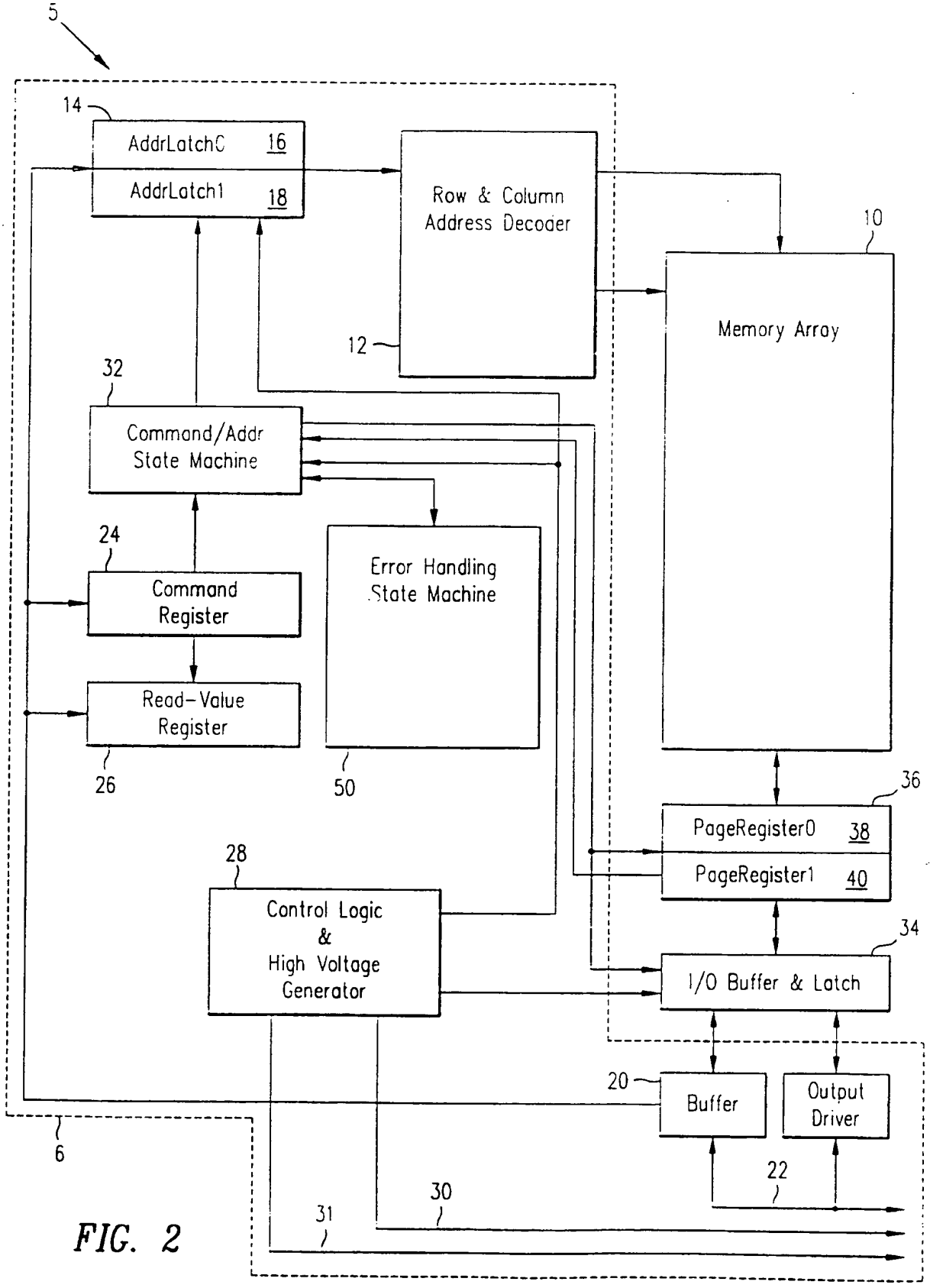
5
14
AddrLatch0 16
AddrLatch1 18
Row & Column Address Decoder
12
10
Memory Array
32
Command/Addr State Machine
24
Command Register
Read-Value Register
26
Error Handling State Machine
50
36
PageRegister0 38
PageRegister1 40
28
Control Logic & High Voltage Generator
34
I/O Buffer & Latch
20
Buffer
Output Driver
22
6
30
31

FIG. 2

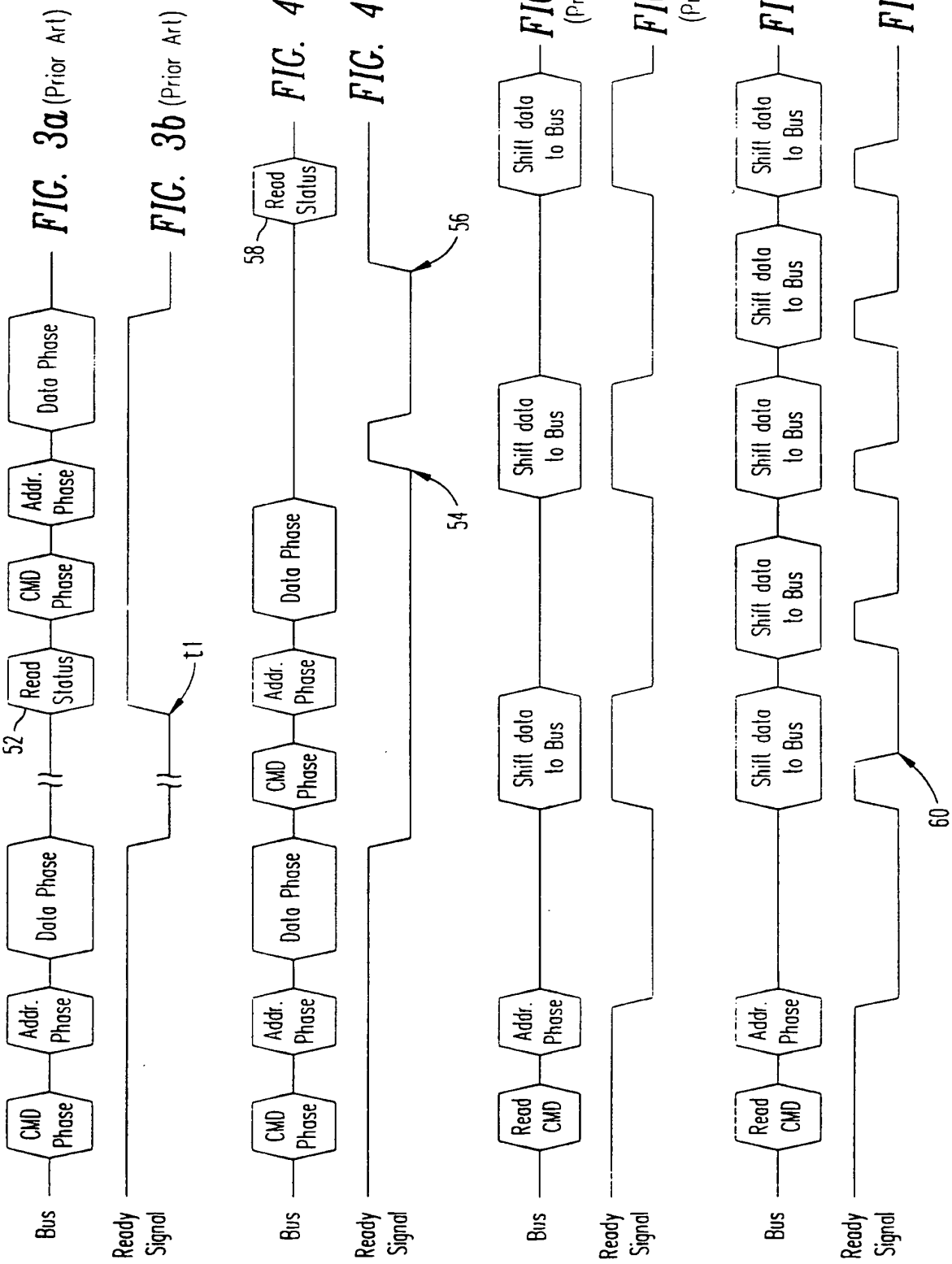

FIG. 3a (Prior Art)

FIG. 3b (Prior Art)

FIG. 4a

FIG. 4b

FIG. 5a (Prior Art)

FIG. 5b (Prior Art)

FIG. 6a

FIG. 6b

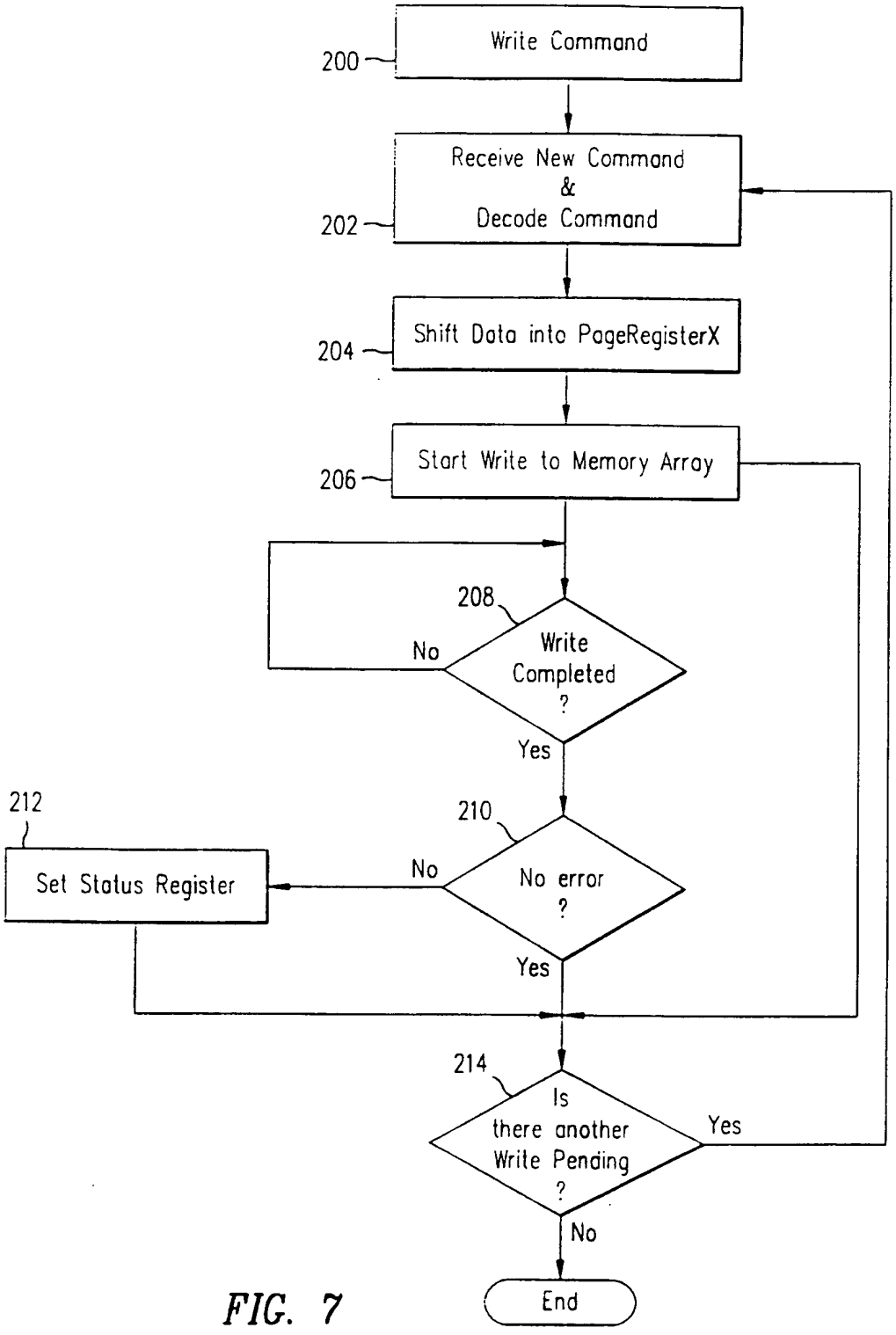
Write Command
200
Receive New Command & Decode Command
202
Shift Data into PageRegisterX
204
Start Write to Memory Array
206
208
Write Completed ?
No
Yes
210
No error ?
No
Yes
212
Set Status Register
214
Is there another Write Pending ?
Yes
No
End

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/27156

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G11C 7/00, 8/00, 16/04
US CL :365/221, 239, 233, 238.5, 185.33
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/221, 239, 233, 238.5, 185.33

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST
pipelin$ or (pipe-lin$) or (pipe lin$)
output$ near3 registers

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,831,929 A (MANNING) 03 November 1998 (03.11.98), figs. 2-4, col. 4, lines 18-63.	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 27 JANUARY 2000	Date of mailing of the international search report 16 FEB 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer VANTHU NGUYEN Telephone No. (703) 308-0956

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